REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-29 in the application. In the present response, the Applicant has amended Claims 1-2 and 26 solely in response to a pending objection to these claims and only to place the application in better condition for allowance. No other claims have been canceled or added. Accordingly, Claims 1-29 are currently pending in the application.

I. Formal Matters and Objections

The Examine has objected to Claims 1-2 and 26 as containing informalities. As noted above, the Applicant has, in response, amended these claims to correct these inadvertent errors and appreciates the Examiner's diligence in finding and bringing them to his attention. Accordingly, the Applicant respectfully requests the Examiner to withdraw the objection to Claims 1-2 and 26 and allow issuance thereof.

II. Rejection of Claims 1-3, 6-10, 12 14, 16-17, 19, and 21-29 under 35 U.S.C. §103

The Examiner has rejected Claims 1-3, 6-10, 12 14, 16-17, 19, and 21-29 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 7,234,042 to Wilson (hereinafter "Wilson") in view of U.S. Patent No. 6,292,845 to Fleck, *et al.* (hereinafter "Fleck"). The Applicant respectfully disagrees.

At item 4 at the bottom of page 3 of the Office Action, the Examiner states:

> ...(b) a first processing channel (Wilson; Figure 1 Items 6_x and 8_x) comprising a plurality of functional units (Wilson; Figure 1 Items 6_x and 8_x) and operable to perform control processing operations (Wilson; Col 4 Lines 7-10);...

In Wilson, a first processing channel (*e.g.*, 6_x, 8_x) cannot, by itself, perform "control processing operations." In Wilson, "control processing operations" – referred to as "special operations" and including, for example, branches, are implemented using a long instruction format which utilizes both the X and Y processing channels. Thus, in Wilson, neither the X channel nor the Y channel can, itself, perform "control processing operations."

The Examiner alleges that in Wilson, the decode unit is operable to detect if each instruction packet is of a first class which defines (i) at least two control instructions. The Examiner equates these to load/store operations. The load/store operations in Wilson are not performed by control instructions – in Wilson, the control operations (special operations) are performed by the long instruction format L1. The load/store operations in Wilson which can be identified in the dual instruction format are memory access operations – see, for example, column 2, line 33.

The load/store operations in Wilson do not anticipate Applicant's "control instructions." Control instructions are defined in the present application at the foot of page 8 as follows: "Herein, "control instructions" include instructions dedicated to program flow, and branch and address generation; but not data processing."

In Wilson, control instructions are implemented using the long instruction format – the dual instruction format is restricted to data processing operations and memory access operations. Control instructions of the present invention are distinct from memory instructions – see, for example, page 9, first full paragraph which refers to 34-bit data instructions (d34), memory-class instructions (m28), and 21-bit control instructions (c21).

The Examiner acknowledges that Wilson does not tech wherein the decode unit detects that the instructions packet comprises at least two control instructions, said control instructions are supplied to the first processing channel for execution in program order.

The Examiner is correct about this. What Wilson teaches is that an instruction packet with at least two instructions in it (note that Wilson does not disclose at least two **control** instructions), these instructions are executed in parallel. This is important when considering the question of obviousness which will be discussed later.

The Examiner alleges that Fleck teaches wherein when two control instructions follow one another, the decode unit issues them to a first processing channel in program order. In Fleck, an instruction load unit loads individual instructions into an instruction buffer, multiple instructions at a time. The type of each respective instruction is indicated (*see, e.g.*, line 25 of column 3). Lines 47-52 of column 3 of Fleck state:

> If two instructions of the same kind follow each other, then multiplexer 4 issues only one single instruction to one of each following pipeline structures 8, 10 or 9, 11. In this case, multiplexer 4 selects a no operation instruction from control lines 12 or 13 for the respective other pipeline structure.

In Fleck, this task is carried out by multiplexer 4 upstream of decode units (8, 9). Thus, Fleck does not disclose "when the decode unit detects that the instruction packet...said control instructions are supplied...for execution in program order."

The decode unit of Fleck does not carry out this function.

The Examiner suggests it would have been obvious to one of ordinary skill to have modified the teachings of Wilson to include processing the control instructions in program order because doing so is easily implemented.

The reference to ease of implementation in Fleck is made at column 3, lines 59 to 61 and is in a different context. It is in the context of being able to provide instructions **in parallel** to the first and second pipeline structures (see column 3, line 53/54). If they cannot be issued in parallel, only a single instruction is issued.

This is the heart of Fleck's teaching. That is, in Fleck, if two instructions of the same kind are in the instruction buffer at the same time, **the cannot** be issued in parallel to the first and second pipeline structures, because one pipeline structure handles one type of instructions and the other pipeline structure handles another type of instruction. In this situation, Fleck has no choice other than to issue a no op instruction for the other pipeline structure. This is clearly disadvantageous because no op instructions waste code density and processor resource. Thus, one of ordinary skill would seek to avoid a situation where no op instructions are needed and would not be induced to follow this part of the teaching of Fleck for that reason.

Furthermore, the teachings of Fleck and Wilson are incompatible in this respect. Wilson clearly discloses the concept of instruction "packets" and "packet types". In Wilson, if a packet type is identified as having two instructions, these instructions are supplied to the data processing channels in parallel – see, for example, column 6, lines 38 to 41 and column 1, lines 63 to 67. This is regardless of the nature of the individual instructions within the packet – dual instruction packets with load store instructions and/or with data processing instructions are all treated in the same way according to Wilson. Thus, there is no motivation in Wilson to take one particular type of dual operation packet and treat it differently to another type of dual instruction packet. Fleck does not teach anything about packets – instructions are handled at an individual level. Teachings which are

applied to the handling of instructions at an individual level and teachings which are applied to the handling of packet types are incompatible.

That is, it would not have been obvious to one of ordinary skill to overturn the teachings of Wilson which define the way in which particular packet types are handled to follow the teachings of Fleck which handles instructions by individual instruction types.

Furthermore, as explained above, Wilson does not disclose a packet of a first class which defines two control instructions. In Wilson, control instructions are implemented using the long format L1 and not the dual operation format. Thus, no teachings are supplied to a skilled person either from Wilson or Fleck concerning the supply of control instructions in program order.

It appears the Examiner must be applying hindsight to reach his conclusion of obviousness. In Wilson, a dual operation instruction could include two load/store operations or two data processing operations. The packet is handled the same way in both cases. In order, therefore, for the Examiner to choose the type of packet including load store operations and suggest that these could be handled differently without any teaching or suggestion in Wilson to this effect, he must be looking at the claim language of the present application. Wilson does not teach a difference between these two kinds of instructions within a dual instruction packet.

Moreover, Fleck does not make any distinction between control instructions or data manipulation instructions as regards how they are treated by the multiplexer. Fleck makes a general comment "if two instructions of the same kind..." this comment applying to any type of instruction and not singling out control instructions. Once again, therefore, there is no teaching or motivation to a skilled person in Fleck to consider that control instructions should be handled differently than any other type of instruction when considering their processing order.

Thus, we submit that the Examiner can only have reached his conclusion as to obviousness by considering the claim language of the present application, applying it to Wilson and then looking for an omitted feature in another piece of prior art. We suggest that this is not a proper basis for an obviousness rejection. Absent the claim language, there is no motivation for a skilled person to make the particular selection that the Examiner makes.

The Examiner does not make a separate rejection of claim 26, although this claim is directed to a method. Based on the foregoing, we submit that Wilson does not disclose:

> "Decoding each instruction packet in turn at a decode unit by determining if the instruction packet is of a first class [note Examiner's correction required] which defines (i) at least two control instructions";
>
> or "wherein when the decode unit detects that the instruction packet comprises at least two control instructions, supplying said at least two control instructions to said first processing channel for execution in sequence". We submit that this latter feature is not Fleck, because in Fleck, the decode unit does not detect that an instruction packet comprises at least two control instructions.

Nor would it be obvious to apply Fleck to Wilson in the manner suggested by the Examiner because Wilson does not make any distinction between a dual instruction packet which contains two load store operations and a dual instruction packet which contains two data processing operations. These packets are considered to be of the same type and are treated in the same way – both supplying their instructions in parallel to the X and Y channels.

Fleck does not teach instruction packets. Fleck states "If two instructions of the same kind follow each other, then multiplexer 4 issues only one single instruction to one of each following

pipeline structures...". Fleck does not make a distinction between control instructions following one another or data processing instructions following one another.

Thus, the rejection of the claim based on obviousness in view of Wilson and Fleck can only be made based on hindsight with the claim language to select the particular parts of Fleck and Wilson.

For at least the reasons given above, the cited portions of the cited combination of Wilson and Fleck, as applied by the Examiner, do not provide a *prima facie* case of obviousness for independent Claims 1, 26, and 29 and Claims that depend thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 1-3, 6-10, 12 14, 16-17, 19, and 21-29 and allow issuance thereof.

III. Rejection of Claims 4-5, 11, 13, 15, 18, and 20 under 35 U.S.C. §103

The Examiner has rejected Claims 4-5, 11, 13, 15, 18, and 20 under 35 U.S.C. §103(a) as being unpatentable over Wilson in view of Fleck and further in view of: U.S. Patent No. 6,880,150 to Takayama, *et al.* (hereinafter "Takayama") for Claims 4-5 and 11; U.S. Patent No. 5,956,518 to DeHon, *et al.* (hereinafter "DeHon") for Claims 13 and 15; U.S. Patent No. 6,725,357 to Cousin (hereinafter "Cousin") for Claim 18; and a paper entitled "Variable Length Instruction Compression for Area Minimization," by Simonen, *et al.* (hereinafter "Simonen") for Claim 20. The Applicant respectfully disagrees.

As established above, the cited portions of the cited combination of Wilson and Fleck, as applied by the Examiner, do not provide a *prima facie* case of obviousness for independent Claim 1. Takayama, DeHon, Cousin, and Simonen have not been cited to correct the above-noted deficiencies

of the cited combination of Wilson and Fleck but to teach the subject matter of the above-mentioned dependent Claims. As such, the cited portions of the cited combination of Wilson and Fleck in view of Takayama, DeHon, Wilson, Cousin, or Simonen do not provide a *prima facie* case of obviousness for independent Claim 1 and Claims that depend thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 4-5, 11, 13, 15, 18, and 20 and allow issuance thereof.

IV. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-29.

The Applicant requests the Examiner to telephone the undersigned agent of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

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